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Volume 66, Issue 1 • December 2018 • Current Issue

Association for Computing Machinery
ISSN: 0004-5411
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Volume 66, Issue 1
Dec 2018

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SECTION: Computer-aided Verification

SECTION: Concurrent Programming

SECTION: Complexity theory

SECTION: Graph Algorithms

SECTION: Randomized Algorithms and Probabilistic Analysis

RESEARCH-ARTICLE **Engineering with Logic: Rigorous Test-Oracle Specification and Validation for TCP/IP and the Sockets API**

Steve Bishop, Matthew Fairbairn, Hannes Mehnert, Michael Norrish, Tom Ridge, Peter Sewell, + 2

December 2018, pp 1–77 • <https://doi.org/10.1145/3243650>

Conventional computer engineering relies on test-and-debug development processes, with the behavior of common interfaces described (at best) with prose specification documents. But prose specifications cannot be used in test-and-debug development in any ...

SECTION: Concurrent Programming

RESEARCH-ARTICLE **The PCL Theorem: Transactions cannot be Parallel, Consistent, and Live**

Victor Bushkov, Dmytro Dziuma, Panagioti Fatourou, Rachid Guerraoui

December 2018, pp 1–66 • <https://doi.org/10.1145/3266141>

We establish a theorem called the PCL theorem, which states that it is impossible to design a transactional memory algorithm that ensures (1) parallelism, i.e., transactions do not need to synchronize unless they access the same application objects, (2) ...

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SECTION: Concurrent Programming

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The PCL Theorem: Transactions cannot be Parallel, Consistent, and Live

[Victor Bushkov](#), [Dmytro Dziuma](#), [Panagiota Fatourou](#), [Rachid Guerraoui](#)December 2018, pp 1–66 • <https://doi.org/10.1145/3266141>

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SIGACCESS Special Interest Group on Accessibility and Computing 3

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The scope of SIGAI, ACM's Special Interest Group on Artificial Intelligence, consists of the study of intelligence and its realization in computer systems. SIGAI's mission is to promote and support AI-related conferences. Members receive reduced registration rates to all affiliated conferences. Members also receive proceedings from the major SIGAI-sponsored conferences. SIGAI publishes a quarterly newsletter, [AI Matters](#), with ideas and announcements of interest to the AI community.

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[Oliver Reiche](#), [Christof Kobylko](#), [Frank Hannig](#), [Jürgen Teich](#)

Proceedings of the 18th ACM SIGPLAN/SIGBED Conference on Languages, Compilers, and Tools for Embedded Systems • June 2017, pp 21–30 • <https://doi.org/10.1145/3078633.3081039>

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Publication: ACM Transactions on Graphics (TOG) • July 2016 • <https://doi.org/10.1145/2897824.2925952>

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Abstract

The Halide image processing language has proven to be an effective system for authoring high-performance image processing code. Halide programmers need only provide a high-level strategy for mapping an image processing pipeline to a parallel machine (a *schedule*), and the Halide compiler carries out the mechanical task of generating platform-specific code that implements the schedule. Unfortunately, designing high-performance schedules for complex image processing pipelines requires substantial knowledge of modern hardware architecture and code-optimization techniques. In this paper we provide an algorithm for automatically generating high-performance schedules for Halide programs. Our solution extends the function bounds analysis already present in the Halide compiler to automatically perform locality and parallelism-enhancing global program transformations typical of those employed by expert Halide developers. The algorithm does not require costly (and often impractical) auto-tuning, and, in seconds, generates schedules for a broad set of image processing benchmarks that are performance-competitive with, and often better than, schedules manually authored by expert Halide developers on server and mobile CPUs, as well as GPUs.

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Automatically Scheduling Halide Image Processing Pipelines

Ravi Teja Mullapudi*

Andrew Adams[‡]Dillon Sharlet[‡]Jonathan Ragan-Kelley[†]

Kayvon Fatahalian*

*Carnegie Mellon University

[‡]Google[†]Stanford University

Abstract

The Halide image processing language has proven to be an effective system for authoring high-performance image processing code. Halide programmers need only provide a high-level strategy for mapping an image processing pipeline to a parallel machine (a *schedule*), and the Halide compiler carries out the mechanical task of generating platform-specific code that implements the schedule. Unfortunately, designing high-performance schedules for complex image processing pipelines requires substantial knowledge of modern hardware architecture and code-optimization techniques. In this paper we provide an algorithm for automatically generating high-performance schedules for Halide programs. Our solution extends the function bounds analysis already present in the Halide compiler to automatically perform locality and parallelism-enhancing global program transformations typical of those employed by expert Halide developers. The algorithm does not require costly (and often impractical) auto-tuning, and, in seconds, generates schedules for a broad set of image processing benchmarks that are performance-competitive with, and often better than, schedules manually authored by expert Halide developers on server and mobile CPUs, as well as GPUs.

Keywords: image processing, optimizing compilers, Halide

Concepts: •Computing methodologies → Graphics systems and interfaces;

algorithm's execution on a machine (called a *schedule*). The Halide compiler then handles the tedious, mechanical task of generating platform-specific code that implements the schedule (e.g., spawning threads, managing buffers, generating SIMD instructions).

Although Halide provides high-level abstractions for expressing schedules, *designing* schedules that perform well on modern hardware is hard; it requires expertise in modern optimization techniques and hardware architectures. For example, around 70 software engineers at Google currently write image processing algorithms in Halide, but they rely on a much smaller cadre of Halide scheduling experts to produce the most efficient implementations. Further, production image processing pipelines are long and complex, and are difficult to schedule even for the best Halide programmers. Arriving at a good schedule remains a laborious, iterative process of schedule tweaking and performance measurement. Also, in large production pipelines, software engineering considerations (e.g., modularity, code reuse) may preclude experts from having the global program knowledge needed to create optimal schedules.

In this paper we address this problem by providing an algorithm for automatically generating high-performance schedules for Halide programs. Our approach is to leverage the function bounds analysis already present in the Halide compiler to automatically perform locality enhancing global program transformations similar to those employed by expert Halide developers. The algorithm does not require costly (and often impractical) auto-tuning, and, in seconds,

